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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,253	07/14/2003	Sudhakar Kale	884.142US2	1288
21186	7590	07/14/2006	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			TO, TUYEN P	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

This is a response to the communication filed on 06/26/2006. Claims 1-26 are pending.

Applicants' election without traverse of Group II (Claims 8-10 and 23-24) in the reply filed on 06/26/2006 is acknowledged. Claims 1-7, 11-22, and 25-26 have been withdrawn.

Claim Objections

1. Claims 8 and 23 are objected to because of the recited limitation. "the control signals" in claims 8 and 23 lacks of antecedent basis. Appropriate correction is required.

Specification

2. The abstract of the disclosure is objected to because it includes more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-10 and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Odawara et al., "Partition and Placement Technique for CMOS Gate Arrays", IEEE Transactions on Computer-Aid Design, Vol. CAD-6, No.3, May 1987, pages 355-363.

(Claim 8 and similarly recited claim 23)

A computerized method (claim 8)/an article (claim 23) for generating a set of vectors ("location macros", section II) for a logic design through computer-automated operations, the method comprising:

identifying logic for generating at least one control signal and excluding the logic from the set of vectors (Section III A, Fig. 5 (a));

identifying at least one instance of a first template to group as a first vector in the set of vectors by using databus identifiers and the control signals (Fig. 5(a), see *b) Bus-type location macro (BTLM)* and *b) Bus-type location macro extraction* in Section III A, page 357); and

identifying at least one instance of a second template to group as a second vector in the set of vectors by using circuit connectivity and a previously formed vector (Fig. 4, see *a) Vertical-type location macro (VTLM)* and *a) VTML extraction* in Section III A).

(Claim 9 and similarly recited claim 24)

The computerized method/an article of claim 8 and 23 respectively, wherein identifying at least one instance of the second template using circuit connectivity and a previously formed vector is performed after all possible vectors are identified using the databus identifiers and the control signals (Section III A).

(Claim 10)

The computerized method of claim 8 wherein the logic design is for a datapath circuit (Figs 4 and 5, Section III A).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

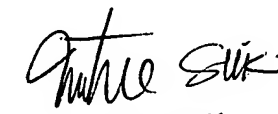
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272- 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Tuyen To

Patent Examiner

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VUTHE SIEK
PRIMARY EXAMINER